CHIPMOS TECHNOLOGIES BERMUDA LTD
Form 6-K
September 05, 2007

SECURITIES AND EXCHANGE COMMISSION

Washington, DC 20549

FORM 6-K

REPORT OF FOREIGN PRIVATE ISSUER

PURSUANT TO RULE 13a-16 OR 15d-16 OF

THE SECURITIES EXCHANGE ACT OF 1934

For the month of September, 2007

ChipMOS TECHNOLOGIES (Bermuda) LTD.

(Translation of Registrant s Name Into English)

11F, No. 3, Lane 91, Dongmei Road

Hsinchu, Taiwan

Republic of China

(Address of Principal Executive Offices)

(Indicate by check mark whether the registrant files or will file annual reports under cover of Form 20-F or Form 40-F.)

Form 20-F ü Form 40-F

(Indicate by check mark whether the registrant by furnishing the information contained in this form is also thereby furnishing the information to the Commission pursuant to Rule 12g3-2(b) under the Securities Exchange Act of 1934.)

Yes No ü

(If Yes is marked, indicate below the file number assigned to the registrant in connection with Rule 12g3-2(b): 82- .)

SIGNATURES

Pursuant to the requirements of the Securities Exchange Act of 1934, the registrant has duly caused this report to be signed on its behalf by the undersigned, thereunto duly authorized.

ChipMOS TECHNOLOGIES (Bermuda) LTD.
(Registrant)

Date: September 5, 2007

By /S/ S. J. Cheng
Name: S. J. Cheng
Title: Chairman & Chief Executive Officer

EXHIBITS

Exhibit Number	
1.1	Press Release
1.2	Patent Summary

Exhibit 1.1

Contacts:

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ChipMOS FILES PATENT INFRINGEMENT SUIT AGAINST WALTON ADVANCED

ENGINEERING INC.

Hsinchu, Taiwan, September 5, 2007 ChipMOS TECHNOLOGIES (Bermuda) LTD. (ChipMOS or the Company) (Nasdaq: IMOS) announced today that its 99.14% owned subsidiary, ChipMOS TECHNOLOGIES INC. (ChipMOS Taiwan) filed a lawsuit on September 5, 2007 Taiwan time in Kaohsiung District Court against Walton Advanced Engineering, Inc. (Walton), alleging infringement by Walton of two of ChipMOS Taiwan s BGA (Ball Grid Array) package related patents which are used for DDR II SDRAM devices.

ChipMOS Taiwan obtained from the retail market several branded memory modules packaged by Walton and sent them to a professional appraisal institution for investigation. ChipMOS Taiwan decided to file the litigation based upon the investigating report of this professional appraisal institution, which concluded that the package device employed on the aforementioned modules infringed ChipMOS Taiwan R.O.C. patent no. 207627 Substrate on Chip Packaging Process and patent no. 207525 Substrate on Chip Packaging Process .

ChipMOS highly values intellectual property while continuously focusing on the R&D of advanced technology and products. As of July 31, 2007, ChipMOS and ChipMOS Taiwan have accumulated 456 registered and active patents, which is a key factor in the Company s leading status of memory and LCD driver SATS (Semiconductor Assembly and Test Services) industry. In order to protect its patents and shareholders rights, ChipMOS Taiwan decided to file the patent infringement lawsuit against Walton, seeking NT$15 million in monetary damages at the initial stage for the losses ChipMOS Taiwan suffered as well as a court order prohibiting Walton from using the allegedly infringing technology.

About ChipMOS TECHNOLOGIES (Bermuda) LTD.:

ChipMOS (http://www.chipmos.com/) is a leading independent provider of semiconductor testing and assembly services to customers in Taiwan, Japan, and the U.S. With advanced facilities in Hsinchu and Southern Taiwan Science Parks in Taiwan and Shanghai, ChipMOS and its subsidiaries provide testing and assembly services to a broad range of customers, including leading fabless semiconductor companies, integrated device manufacturers and independent semiconductor foundries.

Forward-Looking Statements

Certain statements contained in this announcement may be viewed as forward-looking statements within the meaning of Section 27A of the U.S. Securities Act of 1933, as amended, and Section 21E of the U.S. Securities Exchange Act of 1934, as amended. Such forward-looking statements involve known and unknown risks, uncertainties and other factors, which may cause the actual performance, financial condition or results of operations of the Company to be materially different from any future performance, financial condition or results of operations implied by such forward-looking statements. Further information regarding these risks, uncertainties and other factors is included in the Company s most recent Annual Report on Form 20-F filed with the U.S. Securities and Exchange Commission (the SEC) and in the Company s other filings with the SEC.

Exhibit 1.2

Patent Summary

1. Summary: A SOC (Substrate On Chip) packaging process is disclosed. A layer of two-stage thermosetting mixture with solvent is coating on an upside of a substrate. Thereafter, the substrate is heated for removing solvent so that the two stage thermosetting mixture becomes a dry adhesive film without solvent. Thus, the bonding pads of the chip are not covered by the dry adhesive film and a better operating flexibility is obtained in the SOC packaging process.

2. Application: SOC (so called, window BGA or FBGA) packages primarily used for DDR II SDRAM devices.